

Amendments to the Claims:

Please cancel Claims 1 – 3, 5, 6, 10 – 12, 14, and 15; amend Claims 4, 7 – 9, 13, and 16 – 18; and add Claims 19 – 26 as indicated in the following listing of claims, which replaces all prior versions, and listings of claims in the application.

Listing of Claims:

Sub B17

1. – 3. (Canceled).

4. (Currently Amended) A method for synchronizing a digital video host system including a ~~transmitter~~, a receiver[,], circuit and a decoder circuit coupled with the receiver circuit only through a host-system bus, the method comprising:

(a) receiving a first transport packet from ~~the~~ a transmitter with the receiver circuit;

(b) capturing a first system time clock (STC) timestamp at a start of receiving the first transport packet, the first STC timestamp being captured into a latch;

(c) obtaining a program clock reference (PCR) timestamp from the transport packet;

(d) comparing the first STC timestamp to the PCR timestamp to generate a comparison result; ~~and~~

(e) adjusting an STC frequency based on the comparison result in order to maintain synchronization between the receiver circuit and the transmitter;

(f) capturing, with the decoder circuit, a system timestamp for an application system coupled with the decoder circuit but not with the receiver circuit; and

(g) adjusting the system timestamp with an offset based on a message delay time between the decoder circuit and the receiver circuit to maintain synchronization between the decoder circuit and the receiver circuit.

5. – 6. (Canceled).

7. (Currently Amended) The method according to claim 4 further comprising:

(a) receiving data from the decoder circuit into a first register in a bus interface; ~~wherein the decoder is coupled to a communication bus, and where the bus interface couples the receiver to the communication bus~~ comprised by the host-system bus;

(b) latching a second STC timestamp into a second register in the bus interface after receiving the data from the decoder circuit; and

(c) providing the second STC timestamp to the decoder circuit by way of the second register.

8. (Currently Amended) The method according to claim 4 wherein the application system comprises an audio-visual system and the decoder is part of circuit comprises an audio-visual interface.

9. (Currently Amended) The method according to claim 4 wherein the application system comprises a networked computer system and the decoder is part of circuit comprises a computer network interface.

10. – 12. (Canceled).

13. (Currently Amended) A system for synchronizing a digital video host system including a transmitter, receiver[,], circuit and a decoder circuit coupled with the receiver circuit only through a host-system bus, the system comprising:

(a) a parser adapted to obtain a program clock reference (PCR) timestamp from a first transport packet, the first transport packet including the PCR timestamp;

(b) a first latch coupled to the parser, the first latch being adapted to capture a first system time clock (STC) timestamp near a beginning of receipt of a first transport packet from a transmitter by the receiver circuit;

(c) a comparison device coupled to the parser and to the latch, the comparison device being configured to compare the STC timestamp to the PCR timestamp so as to generate a comparison result; ~~and~~

(d) a first adjuster coupled to the comparison device, the first adjuster being adapted to adjust a frequency of the system time clock based on the comparison result in order to maintain the synchronization between the receiver circuit and the transmitter;

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cont.*
(e) a second latch in the decoder circuit, the second latch being adapted to capture a system timestamp for an application system coupled with the decoder circuit but not with the receiver circuit; and

(f) a second adjuster coupled to the decoder circuit, the second adjuster being adapted to adjust the system timestamp with an offset based on a message delay time between the decoder circuit and the receiver circuit to maintain synchronization between the decoder circuit and the receiver circuit.

14. – 15. (Canceled).

16. (Currently Amended) The system according to claim 13 further comprising:

(a) a first register in a bus interface comprised by the host-system bus, the first register being adapted to receive data from the decoder circuit, ~~where the decoder is coupled to a communication bus, and where the bus interface couples the receiver to the communication bus;~~ and

(b) a second register in the bus interface, the second register being adapted to latch a second STC timestamp after the first register receives the data from the decoder circuit,

wherein the second STC timestamp is provided to the decoder circuit by way of the second register.

17. (Currently Amended) The system according to claim 13 wherein the application system comprises an audio-visual system and the decoder is part of circuit comprises an audio-visual interface.

18. (Currently Amended) The system according to claim 13 wherein the application system comprises a networked computer system and the decoder is part of circuit comprises a computer network interface.

19. (New) The method according to claim 4 wherein the offset is scaled by a nonunity value.

20. (New) A method for synchronizing a digital video host system including a receiver circuit and a decoder circuit coupled with the receiver circuit only through a host-system bus, the method comprising:

- (a) receiving a first transport packet from a transmitter with the receiver circuit;
- (b) capturing a first system time clock (STC) timestamp at a start of receiving the first transport packet, the first STC timestamp being captured into a latch;
- (c) obtaining a program clock reference (PCR) timestamp from the transport packet;
- (d) comparing the first STC timestamp to the PCR timestamp to generate a comparison result;
- (e) adjusting an STC frequency based on the comparison result in order to maintain synchronization between the receiver circuit and the transmitter;
- (f) receiving data from the decoder circuit into a first register in a bust interface comprised by the host-system bus;

(g) latching a second STC timestamp into a second register in the bus interface after receiving the data from the decoder circuit; and

(h) providing the second STC timestamp to the decoder circuit by way of the second register.

21. (New) The method according to claim 20 wherein the decoder circuit comprises an audio-visual interface.

22. (New) The method according to claim 20 wherein the decoder circuit comprises a computer network interface.

23. (New) The system according to claim 13 wherein the offset is scaled by a nonunity value.

24. (New) A system for synchronizing a digital video host system including a receiver circuit and a decoder circuit coupled with the receiver circuit only through a host-system bus, the system comprising:

(a) a parser adapted to obtain a program clock reference (PCR) timestamp from a first transport packet, the first transport packet including the PCR timestamp;

(b) a first latch coupled to the parser, the first latch being adapted to capture a first system time clock (STC) timestamp near a beginning of receipt of a first transport packet from a transmitter by the receiver circuit;

(c) a comparison device coupled to the parser and to the latch, the comparison device being configured to compare the STC timestamp to the PCR timestamp so as to generate a comparison result;

(d) a first adjuster coupled to the comparison device, the first adjuster being adapted to adjust a frequency of the system time clock based on the comparison result in order to maintain the synchronization between the receiver circuit and the transmitter;

(e) a first register in a bust interface comprised by the host-system bus, the first register being adapted to receive data from the decoder circuit; and

(f) a second register in the bus interface, the second register being adapted to latch a second STC timestamp after the first register receives the data from the decoder circuit, wherein the second STC timestamp is provided to the decoder circuit by way of the second register.

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concl.* 25. (New) The system according to claim 24 wherein the decoder circuit comprises an audio-visual interface.

26. (New) The system according to claim 24 wherein the decoder circuit comprises a computer network interface.
